A C-Band 4-Stage Low Noise Miniaturized Amplifier Using Lumped Elements

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ABSTRACT

A C-band monolithic four-stage low noise miniaturized amplifier has been developed. It employs lumped elements for the matching circuit to reduce the chip size. In the design of the IC, an integrated CAD system was used to consider parasitic microwave components. The 1.65 mm × 2.30 mm amplifier achieved a gain of over 40 dB with a noise figure of less than 1.7 dB. The amplifier gives a minimum noise figure of 1.54 dB and a gain of 41 dB. A good agreement between measured and simulated data has been achieved.

INTRODUCTION

There are several papers describing monolithic low noise amplifiers (LNAs)[1-6]. However, Monolithic Microwave Integrated Circuits (MMICs) need to be much more improved in term of low noise performance and cost to surpass hybrid MICs in commercial communication applications. In this paper, we describe an LNA producing a gain of over 40 dB with a noise figure of lower than 1.7 dB with self-aligned multi-layer gate FET's(SAMFET)[7] at C-Band. The amplifier gives a minimum noise figure of 1.54 dB and a gain of 41 dB. The cost of engineering design is also important. To succeed in the first fabrication pass, a newly developed computer aided design is adopted. A good agreement between measured and simulated data has been achieved at the first fabrication pass by considering parasitic microwave components such as bends and tees which are extracted from the physical layout and inductor model. The chip size is as small as 1.65 mm × 2.30 mm.

DEVICE CHARACTERIZATION

Figure 1 shows a cross sectional SEM photograph of the SAMFET[7].

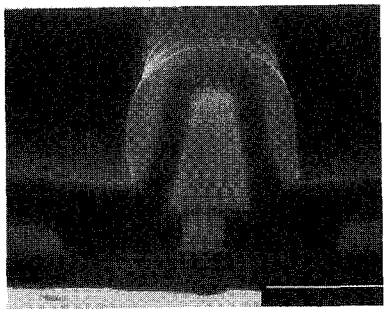

Fig.1. SEM photograph of the SAMFET.

The gate metal consists of two layers. The under

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layer chosen is WSi to obtain good reliability, and the upper layer is Au to obtain low gate resistance. The channel n-layer is formed by selective ion-implantation into a 100 μm thick GaAs substrate. Si is used for the n-layer. WSi gate films are deposited by sputtering. The gate films act as a mask for n^+ and n'-implantation.

Each FET contained in this LNA has a gate size of 0.5 μm × 300 μm. The typical DC characteristics of these devices are an Idss (Vd = 3 V) of 60 mA with a pinch-off voltage of -1.0 V. Figure 2 shows measured maximum stable and available gain (MAG/MSG) versus frequency at Vd = 3 V, Id = 15 mA. The SAMFET has a maximum stable gain up to 20 GHz. An NFmin of 0.6 dB with a Ga of 10.0 dB are obtained at 5 GHz.

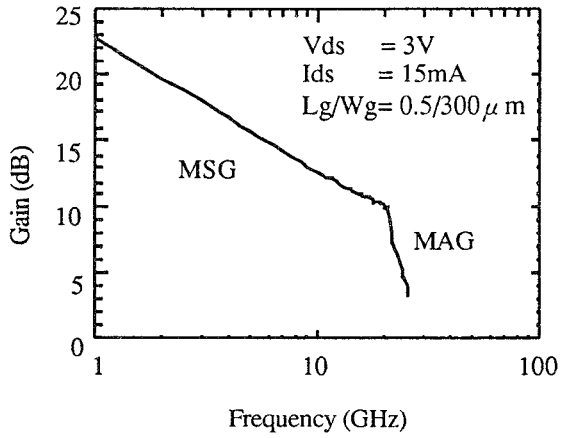


Fig.2. Frequency dependence of the maximum stable and available gain.

CIRCUIT DESIGN

The principal objective was to design an amplifier with a noise figure of lower than 2.0 dB, a gain of 40 dB, VSWR of less than 2. A 4-stage circuit topology was chosen to achieve the target gain. A 0.5 μm × 300 μm SAMFET was used as an active device for each stage at the 4-stage amplifier. Each SAMFET was biased at 3 V and 15 mA of Ids for good noise performance. Due to the difference of the optimum matching point for noise and input VSWR, series inductive feedback of the first-stage FET was used to force the Γopt and S^*_{11} closer. The input, output and inter-stage matching network elements used are only lumped elements for the purpose of miniaturizing the chip size. Also a design with only seven via-holes is used for the same purpose. The inter-stage networks were conjugate-matched using two spiral inductors and one MIM capacitor. The 2 kΩ bias resisters are used as gate bias circuit elements. To obtain circuit stability, a parallel feedback circuit which consists of MIM capacitor and resistor was used on the 2nd and 4th-stage FETs. To reduce loss, the structure of spiral inductor is formed using 5 μm-thickness with width/space of 10/10 μm. Figure 3 shows a circuit diagram of the amplifier consisting of ideal lumped elements.

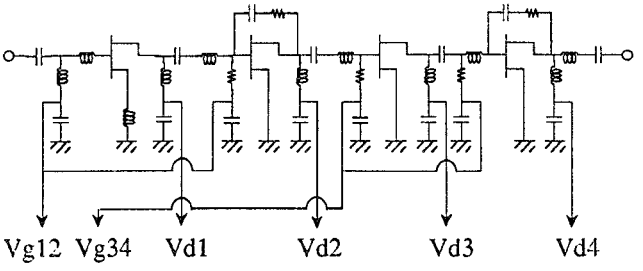
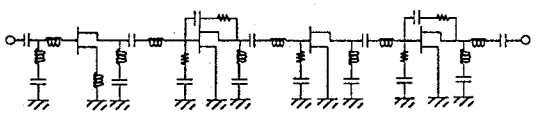


Fig.3. Schematic diagram of the C-band 4-stage LNA MMIC.

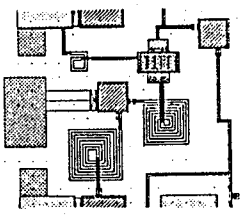
INTEGRATED CAD SYSTEM

Figure 4 shows the 4-stage amplifier designed by using the Integrated CAD system[8]. In the design of

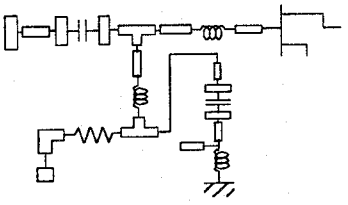
MMICs, it is important to consider parasitic microwave components such as transmission bends and tees. In the figure, (a) is a schematic circuit of ideal circuit elements, (b) is created using a symbolic layout, and (c) is a part of an equivalent circuit which was back-annotated from the symbolic layout in consideration of parasitic microwave components. In order to achieve ideal design characteristics, the inductance parameters are re-optimized and a final layout is created. (d) is the final symbolic layout of the 4-stage low noise amplifier. The symbolic layout was automatically converted into photo mask patterns for fabrication of the MMIC.



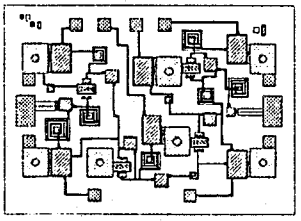
(a) The schematic circuit of ideal circuit elements.



(b) Symbolic layout created for the MMIC.



(c) A part of an equivalent circuit which was used in consideration of parasitic microwave components.



(d) The final symbolic layout of the 4-stage low noise amplifier.

Fig.4. Method of MMIC layout design.

RESULTS

Figure 5 shows a photograph of the amplifier. The chip size is 1.65 mm × 2.30 mm. Figure 6 shows the measured results of the amplifier compared with the designed data. This amplifier achieved a gain of over 40 dB with a noise figure of lower than 1.7 dB. The amplifier gives a minimum noise figure of 1.54 dB and a gain of 41 dB. A good agreement between measured and simulated data has been achieved.

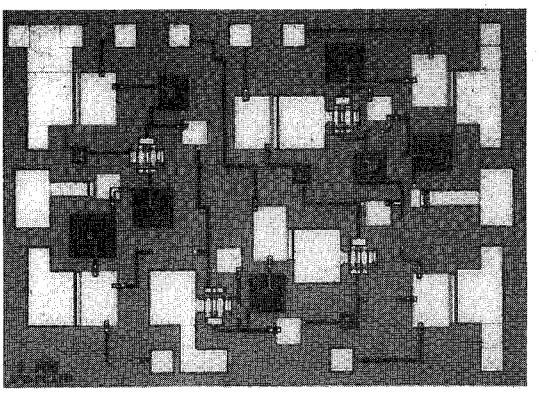
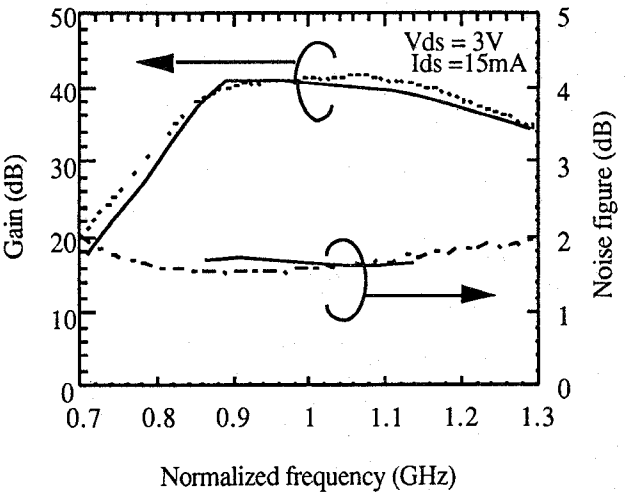
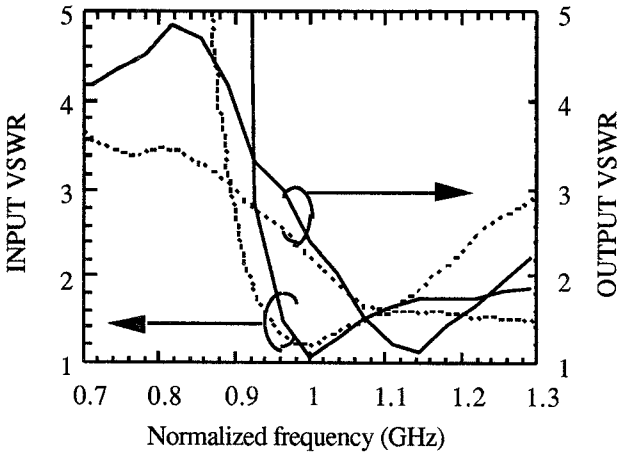


Fig.5. Photograph of the C-band 4-stage LNA MMIC.



(a)



(b)

Fig.6. Comparison between simulation and measurement. (a) Gain and noise figure. (b) Input and output VSWR.

--------- Simulated ——— Measured

CONCLUSION

A C-band monolithic 4-stage low noise miniaturized amplifier has been successfully developed using lumped elements. The 1.65 mm × 2.30 mm amplifier achieved a typical gain of over 40 dB with a typical noise figure of lower than 1.7 dB. The amplifier gives a minimum noise figure of 1.54 dB and a gain of 41 dB. A good agreement between measured and simulated data has been achieved.

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